Characterization of Dielectric Breakdown in High-Voltage GaN MIS-HEMTs

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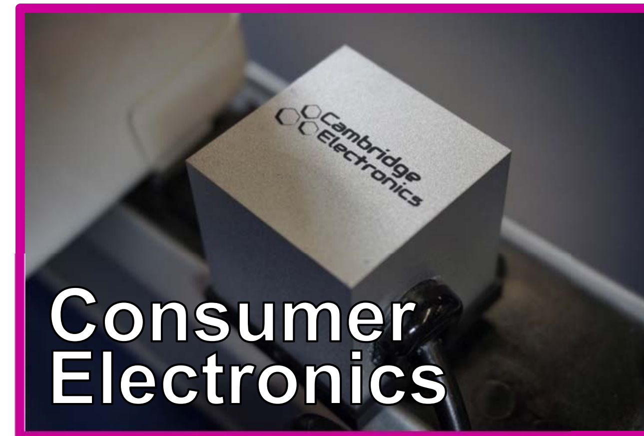
Outline

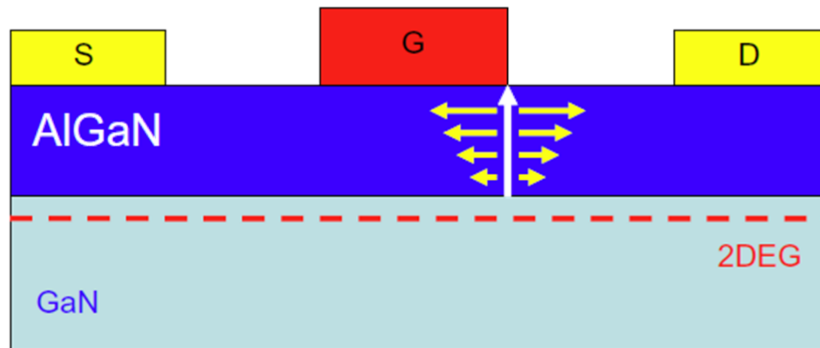
- Motivation & Challenges
- Time-Dependent Dielectric Breakdown (TDDB) Experiments:
  - Current-Voltage
  - Capacitance-Voltage
- Progressive Breakdown
- Conclusions

Motivation

GaN Field-Effect Transistors (FETs) promising for high-voltage power applications → more efficient & smaller footprint

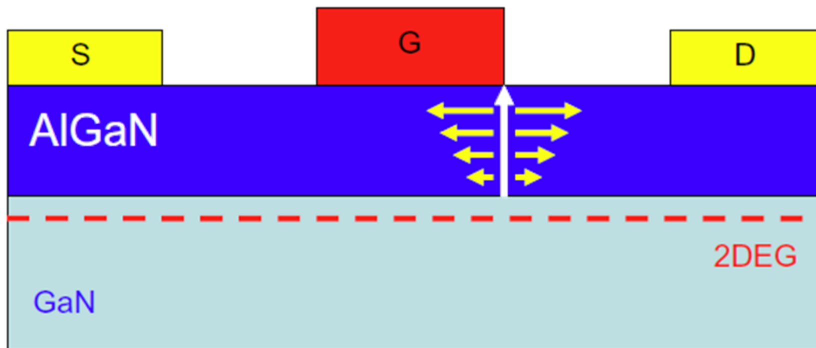


GaN Reliability Challenges



Inverse piezoelectric effect
J. A. del Alamo, MR 2009

GaN Reliability Challenges



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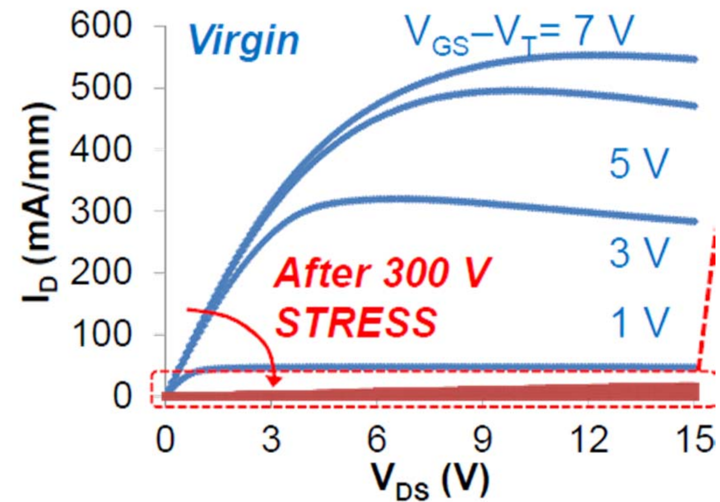
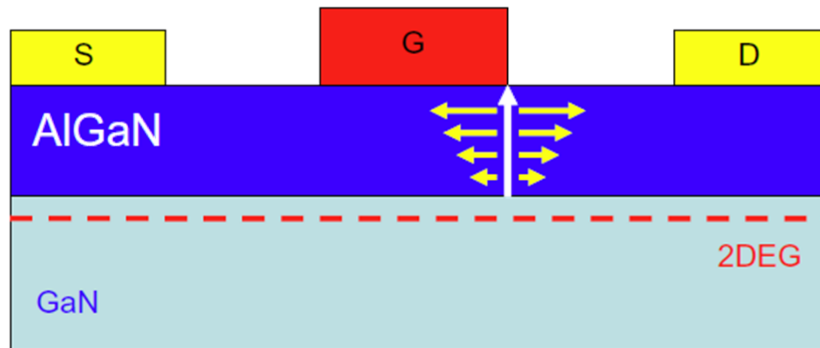


Current collapse
D. Jin, IEDM 2013

GaN Reliability Challenges



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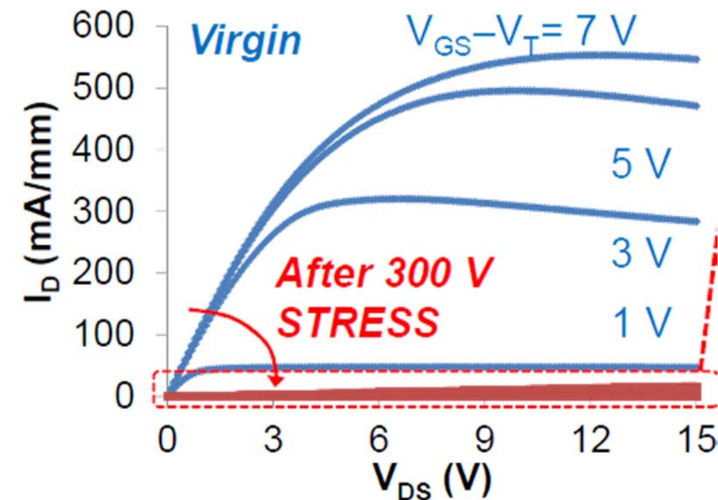

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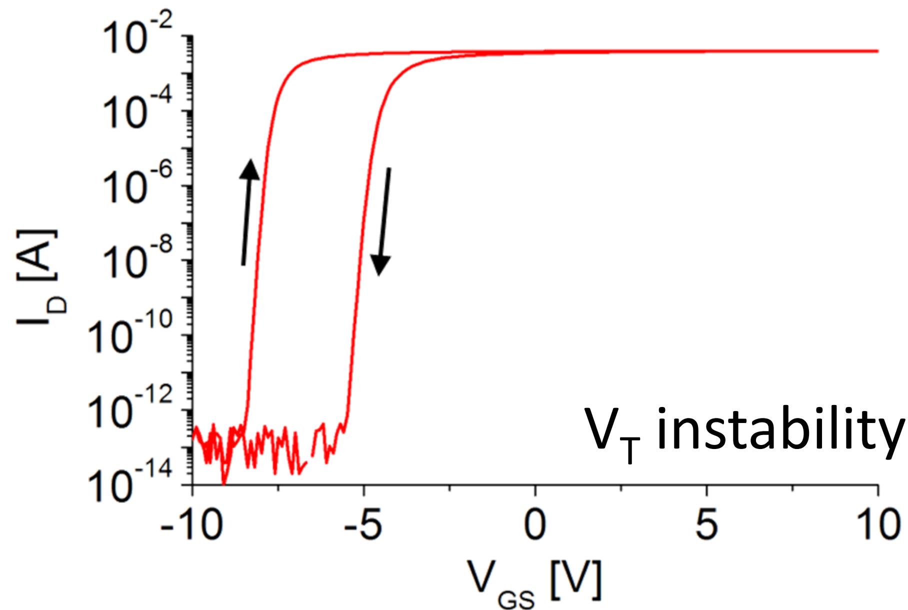
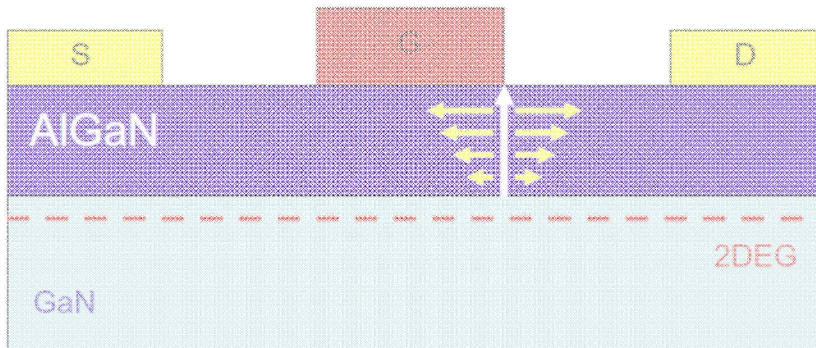


V_T instability

GaN Reliability Challenges



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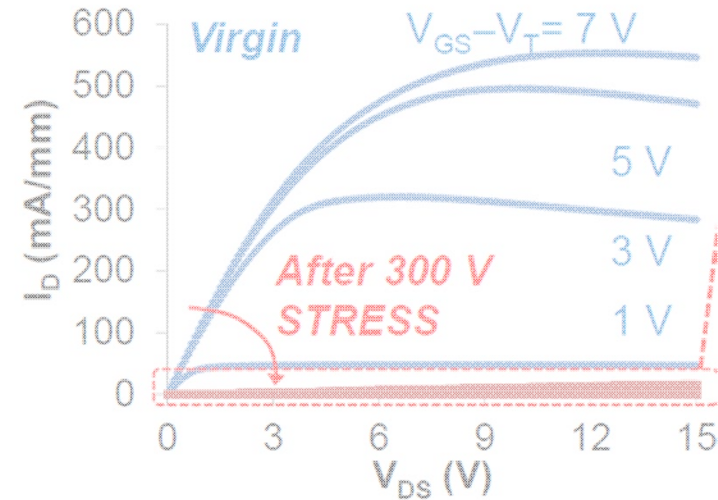

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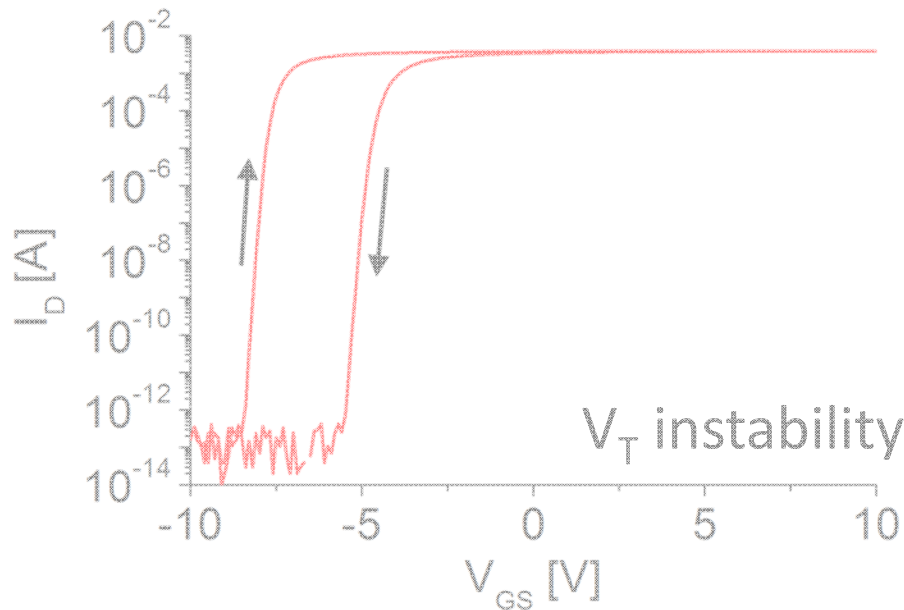
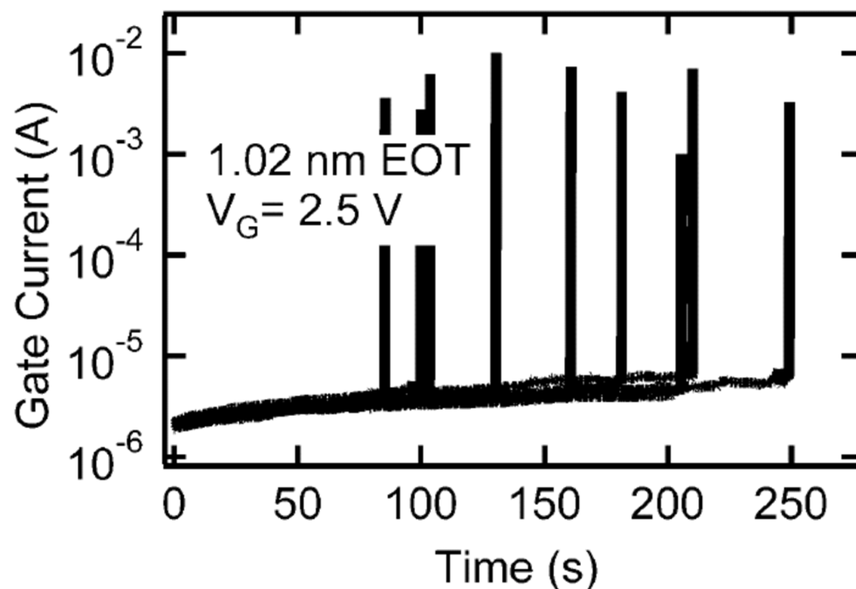


Gate oxide reliability

Time-Dependent Dielectric Breakdown

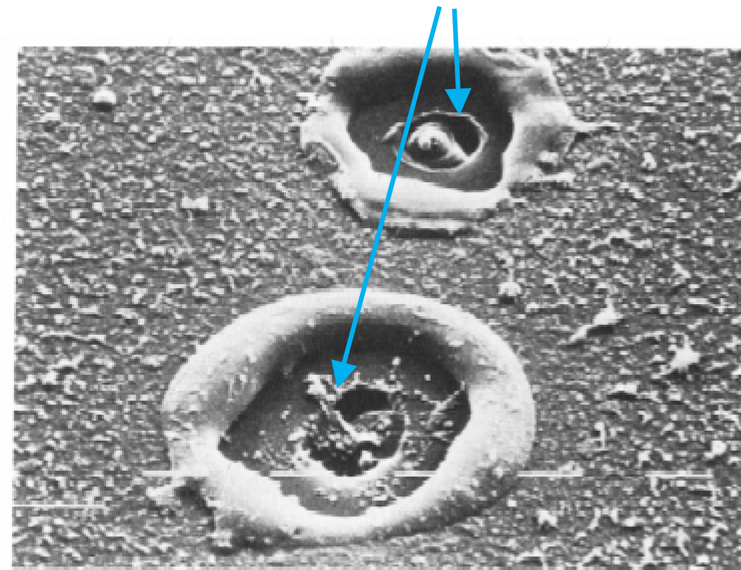
- High gate bias → defect generation → catastrophic oxide breakdown
- Often dictates lifetime of chip

Typical TDDB experiments:
Si high-k MOSFETs



T. Kauerauf, EDL 2005

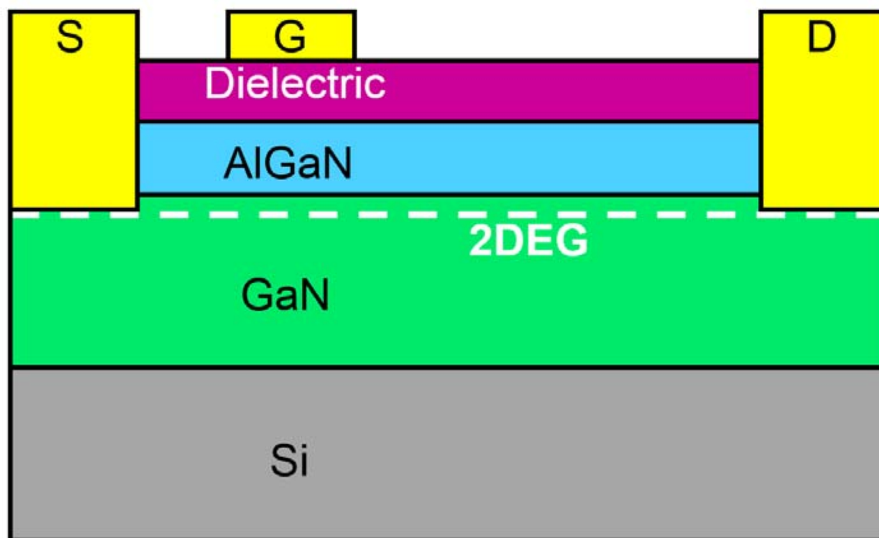
Gate material melted after breakdown

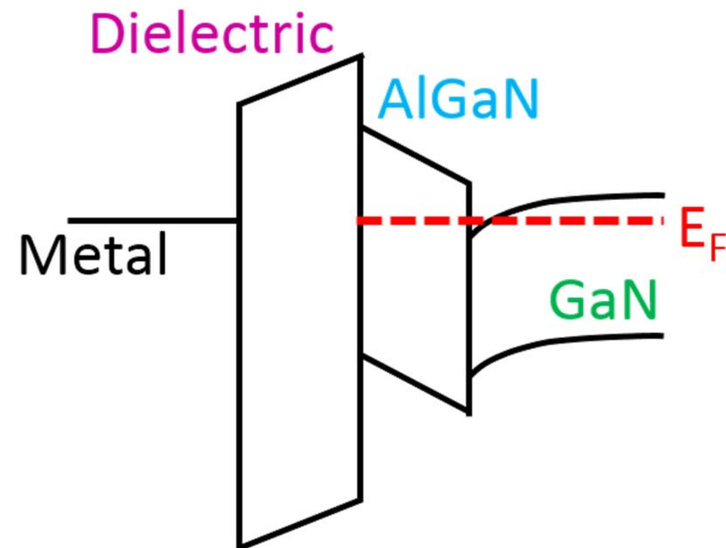


D. R. Wolters, Philips J. Res. 1985

Dielectric Reliability in GaN FETs

AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs)



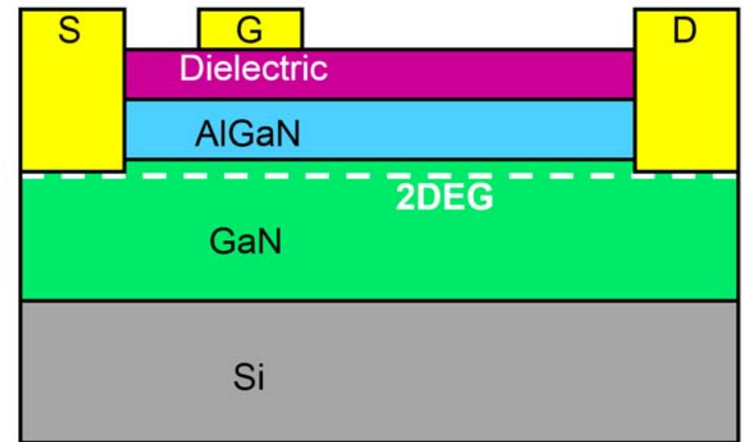


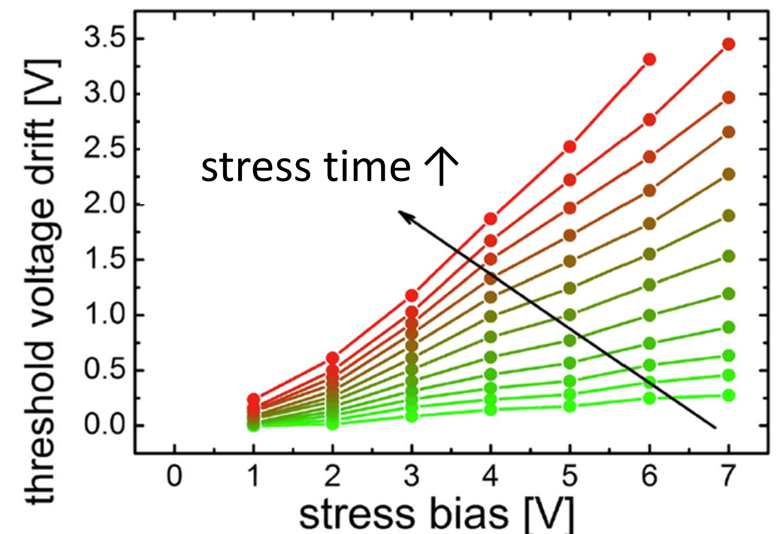
Very little currently known about TDDB in GaN
→ goal of this work

TDDB Experiments: Current-Voltage

GaN MIS-HEMTs for TDDB study

- GaN MIS-HEMTs from industry collaboration: depletion-mode
- Gate stack has multiple layers & interfaces
  - → Uncertain electric field distribution
  - → Many trapping sites
- Complex dynamics involved
  - → Unstable and fast changing V_T

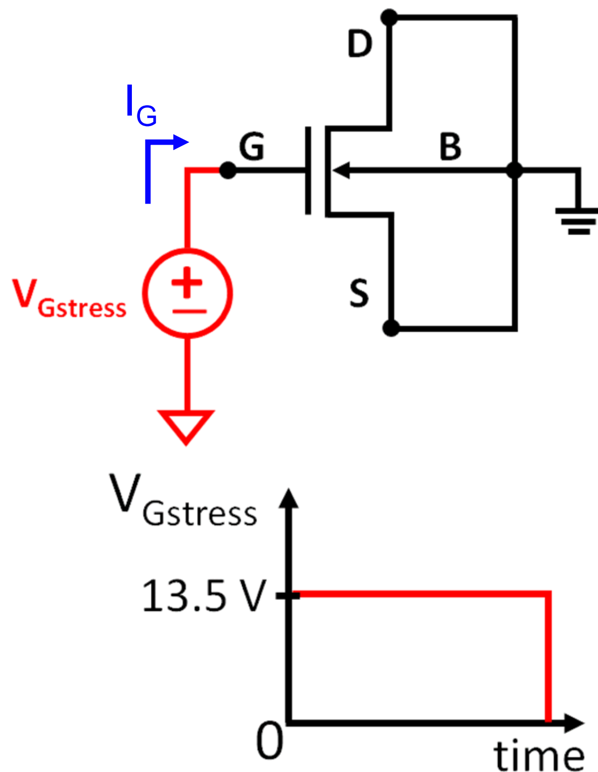


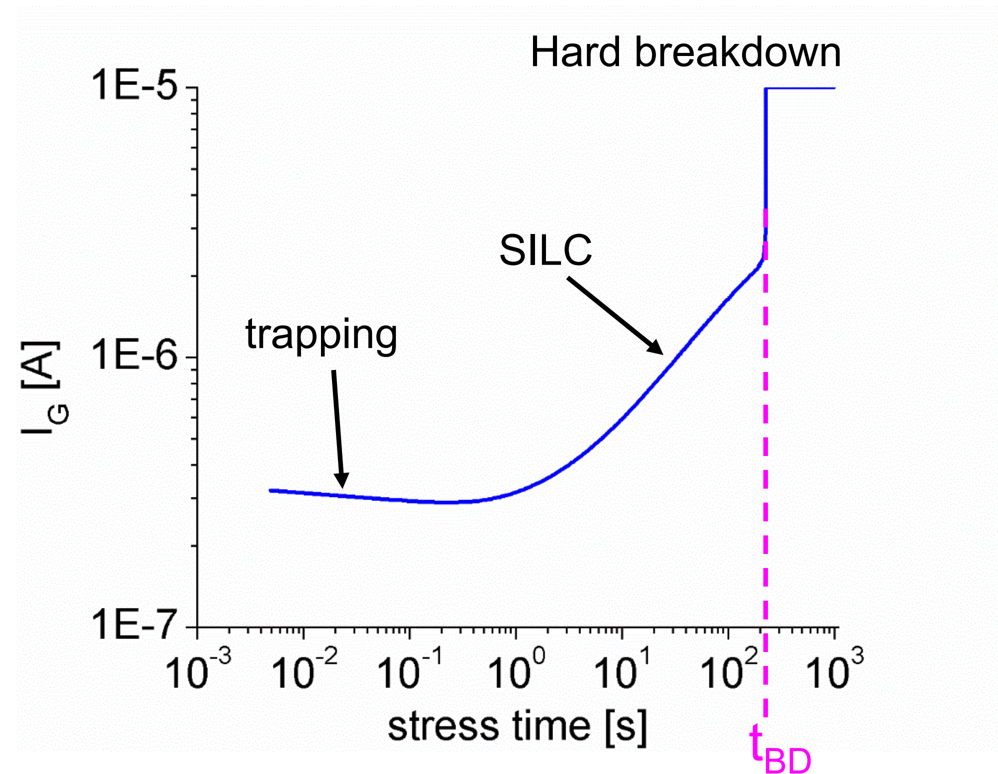


P. Lagger, TED 2014

Classic TDDB Experiment

Constant gate voltage stress experiment:



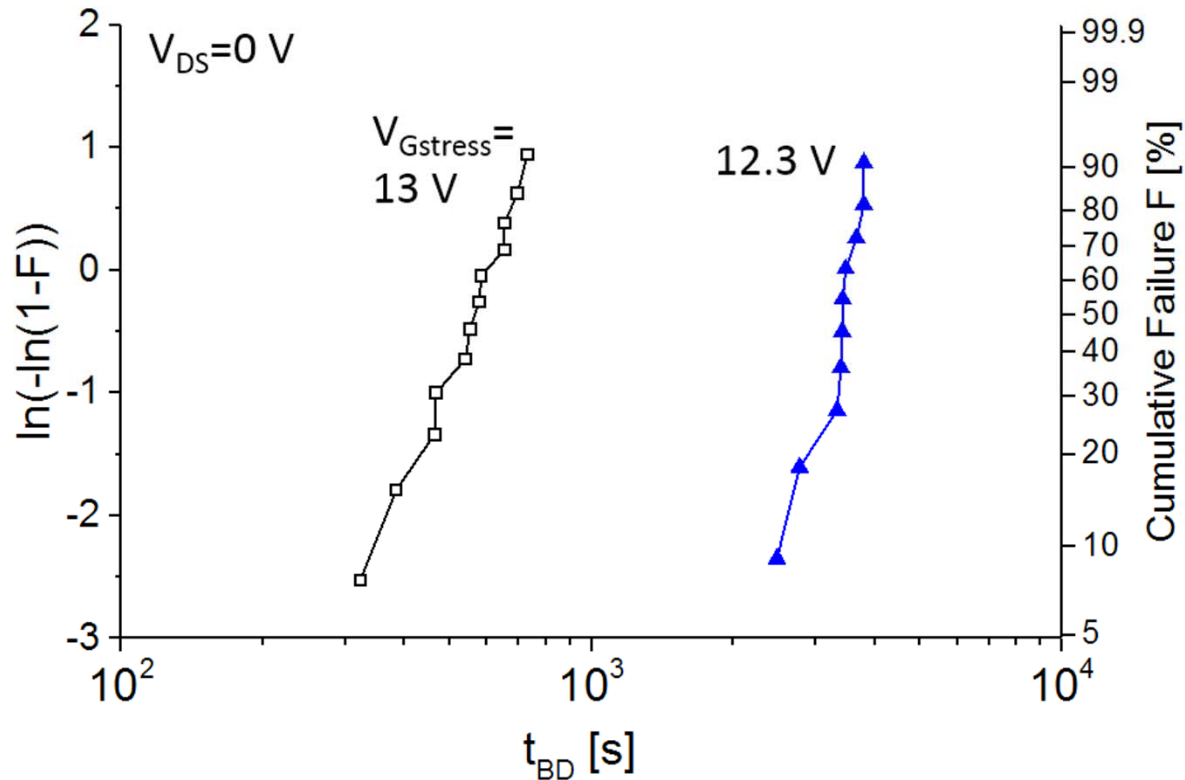


S. Warnock, CS MANTECH 2015

Experiment gives time to breakdown and shows generation of stress-induced leakage current (SILC)

GaN TDDB Statistics

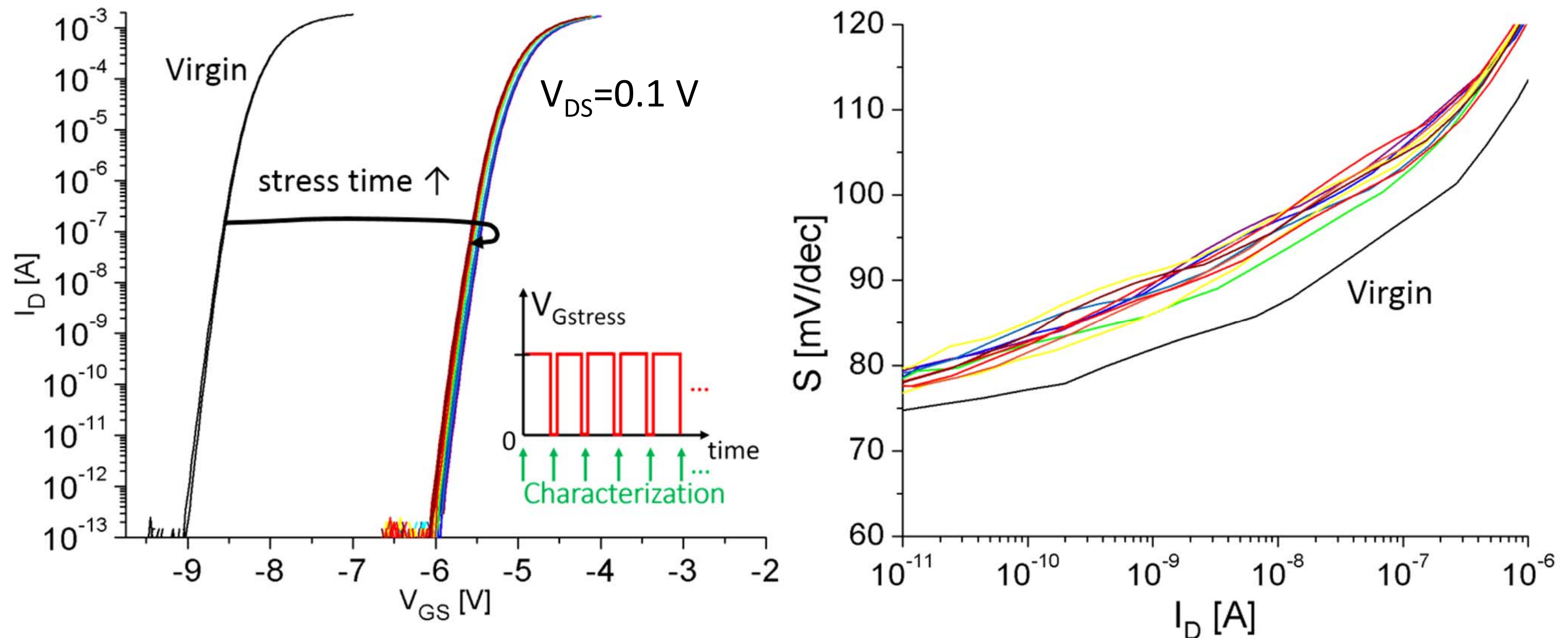
Examine statistics for different $V_{Gstress}$



- Weibull distribution
- As $V_{Gstress}$ ↑, t_{BD} ↓
- Parallel statistics → consistent with results in silicon

TDDB with Periodic Characterization

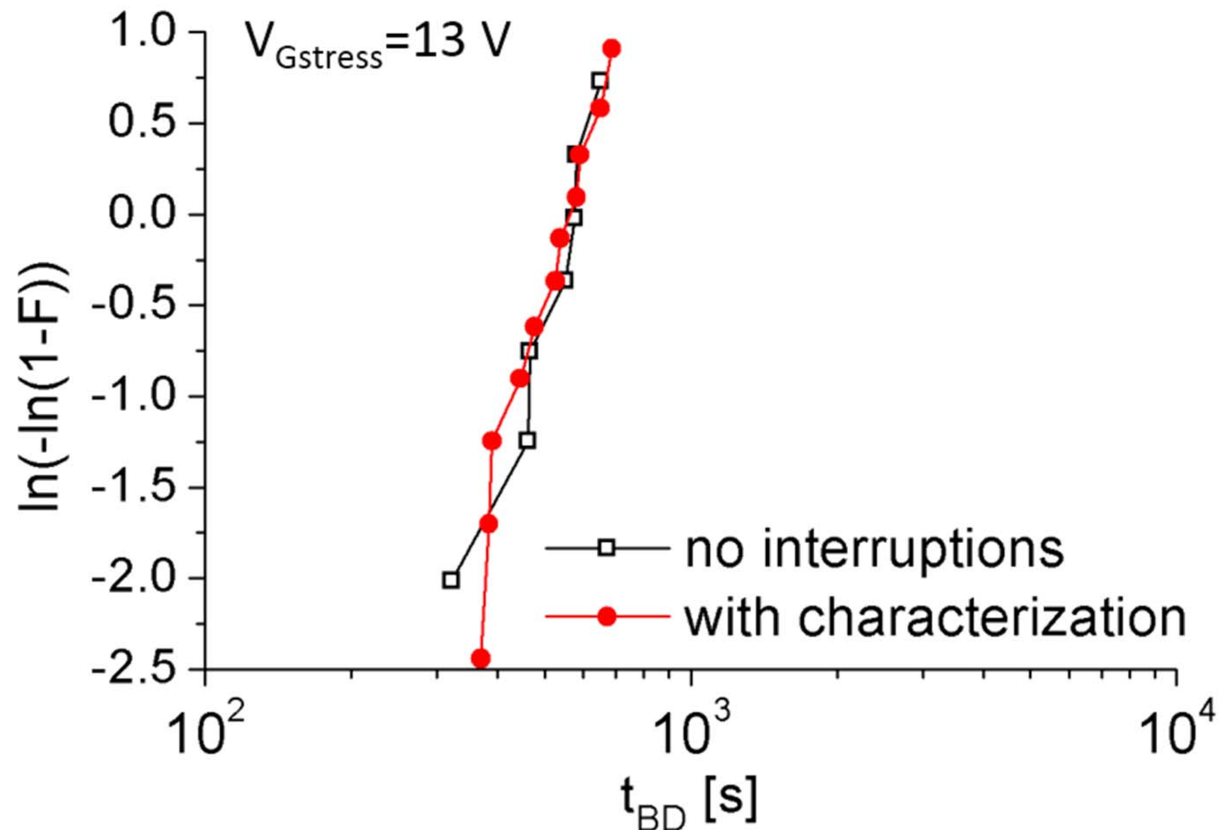
Pause TDDB stress and sweep transfer characteristics at V_{DS}=0.1 V



- Large V_T shift → trapping in dielectric or AlGaN
- Immediate S degradation → interface state generation early in experiment

Validity of Characterization Approach

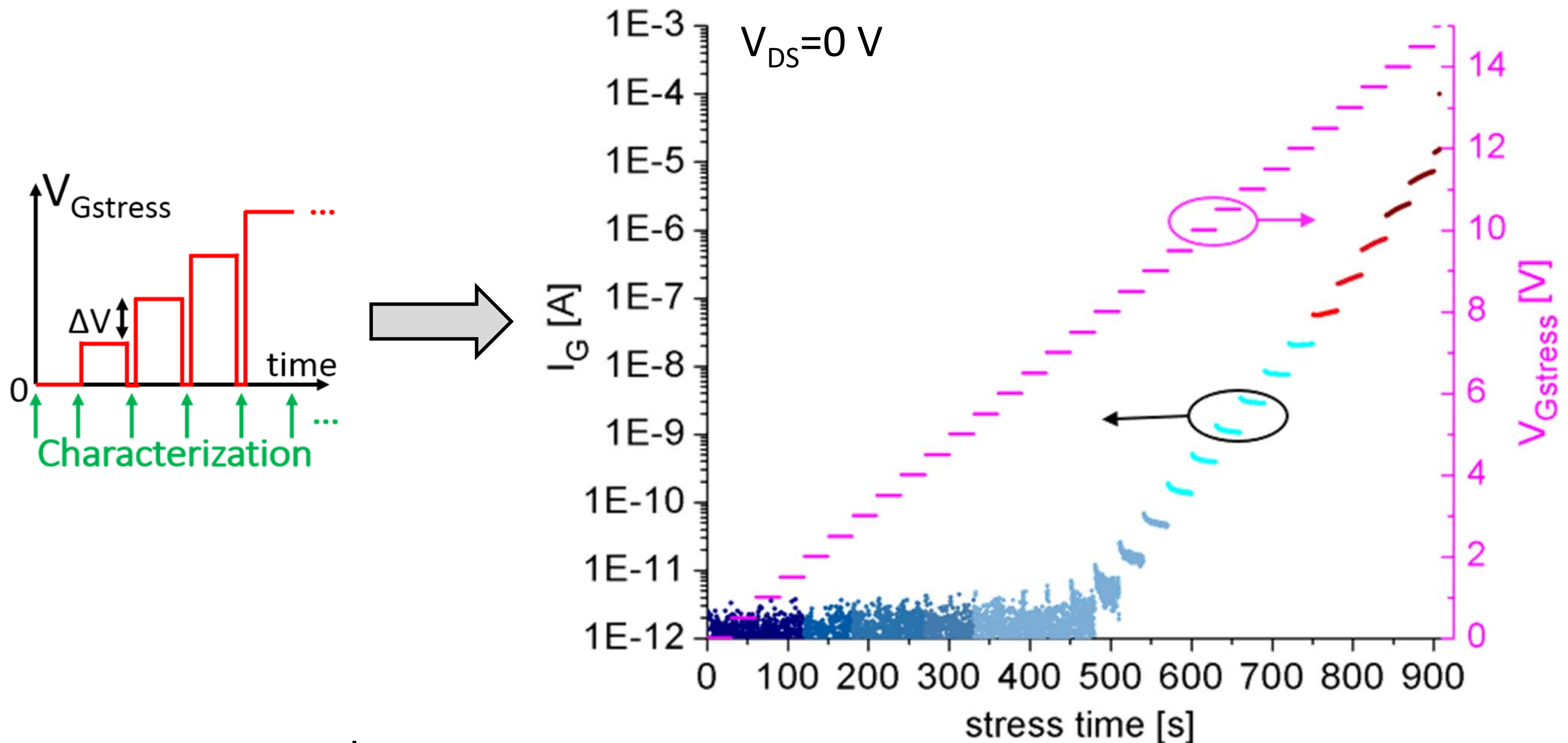
Compare statistics for standard and interrupted schemes



Same statistics for both schemes → characterization is benign

Step-Stress TDDB

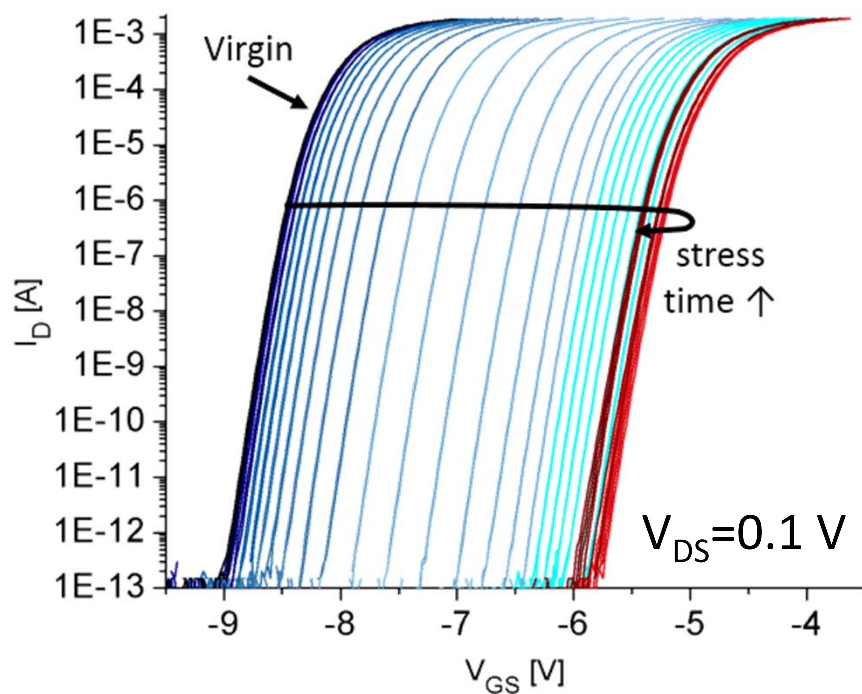
- Step-stress to examine early stages of degradation
- Step $V_{Gstress}$ in 0.5 V increments until breakdown

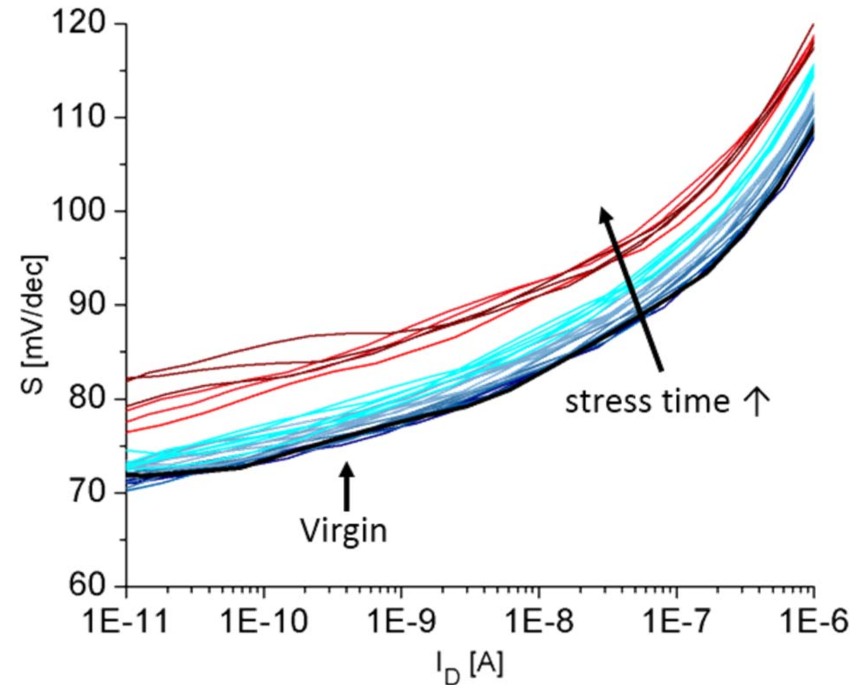


- Low $V_{Gstress}$: I_G ↓ ⇒ trapping
- High $V_{Gstress}$: I_G ↑ ⇒ SILC

Step-Stress TDDB

Transfer characteristics in between stress steps

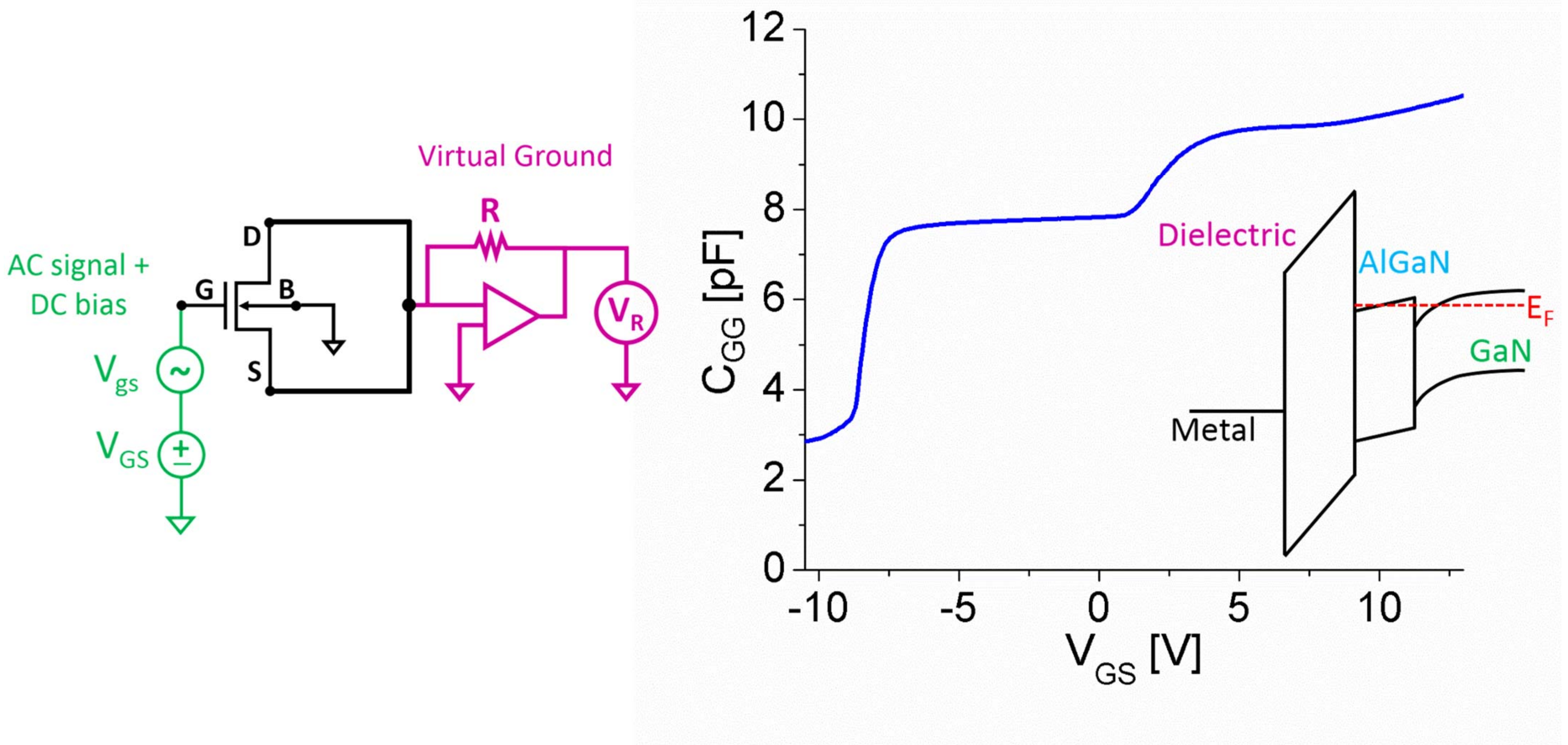




- S and V_T degradation is progressive
- At $V_{Gstress}$ ~12.5 V, ΔV_T < 0 (red lines)
  - Sudden increase in S, appearance of SILC→ interface state generation

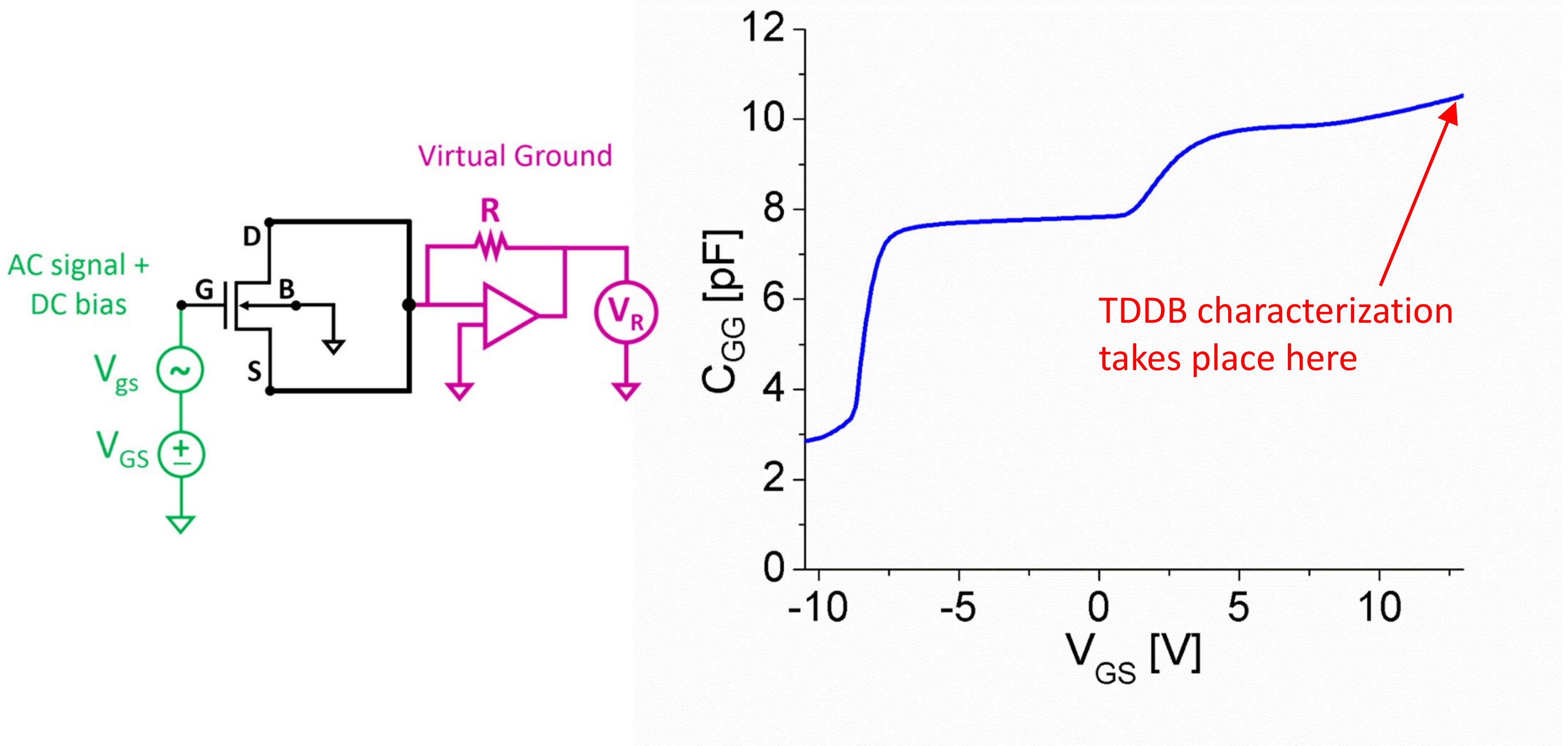
TDDB Experiments: Capacitance-Voltage

C-V Characterization



- At V_{GS}>1 V, conduction band of AlGaN starts being populated

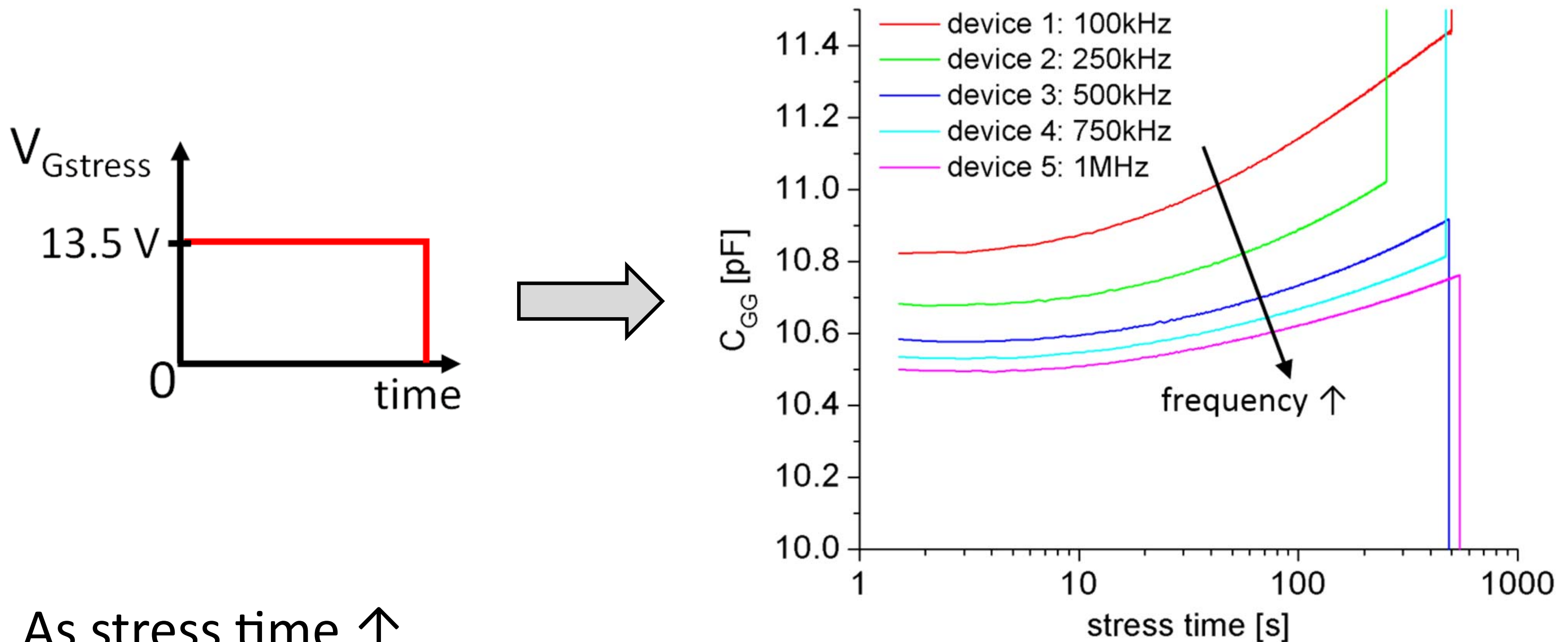
C-V Characterization



- TDDB characterized in regime where AlGaN is populated with electrons

Constant $V_{Gstress}$ TDDB

C_{GG} vs. stress time in 5 devices at 5 different frequencies:

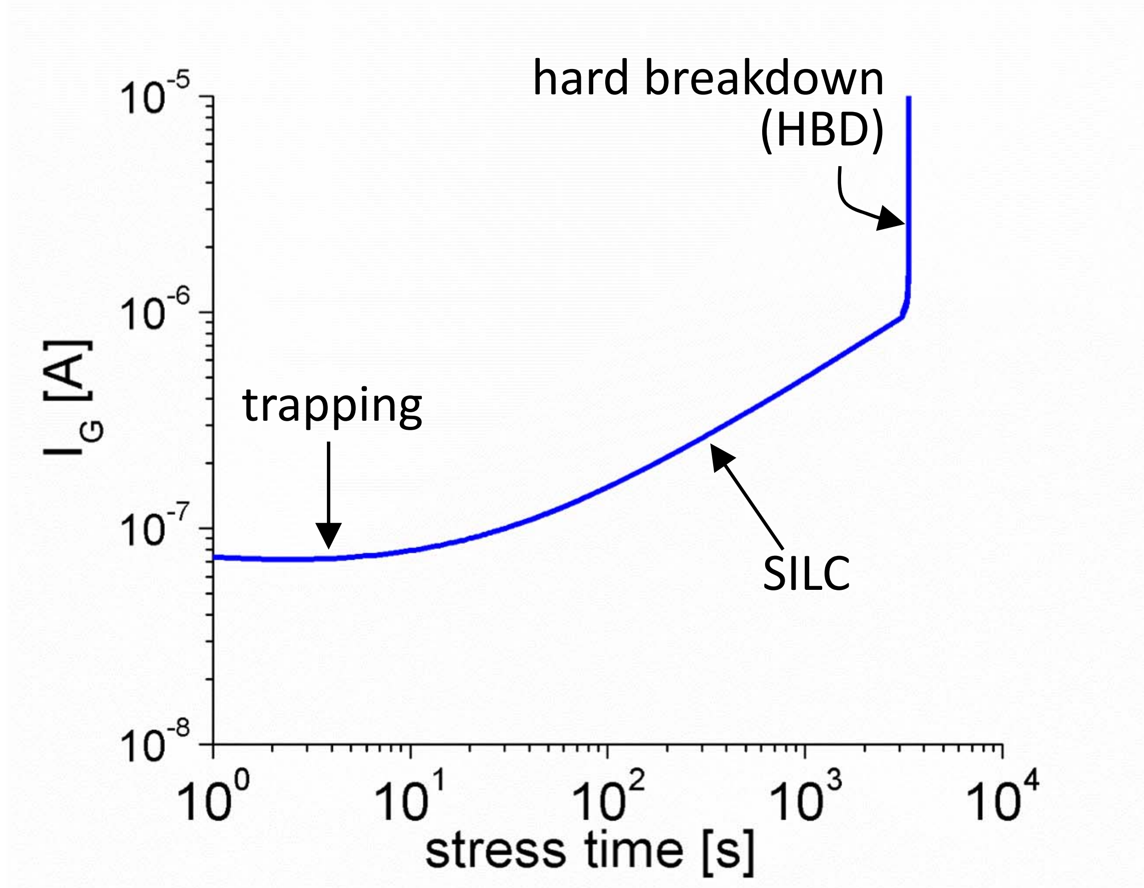


- As stress time ↑
  → C_{GG} ↑
  → Frequency dispersion ↑
- Consistent with trap creation and trapping
  – In dielectric and/or at MIS interface

Progressive Breakdown

Observation of Progressive Breakdown

Revisit classic TDDB experiment: $V_{Gstress}$=12.6 V, V_{DS}=0 V



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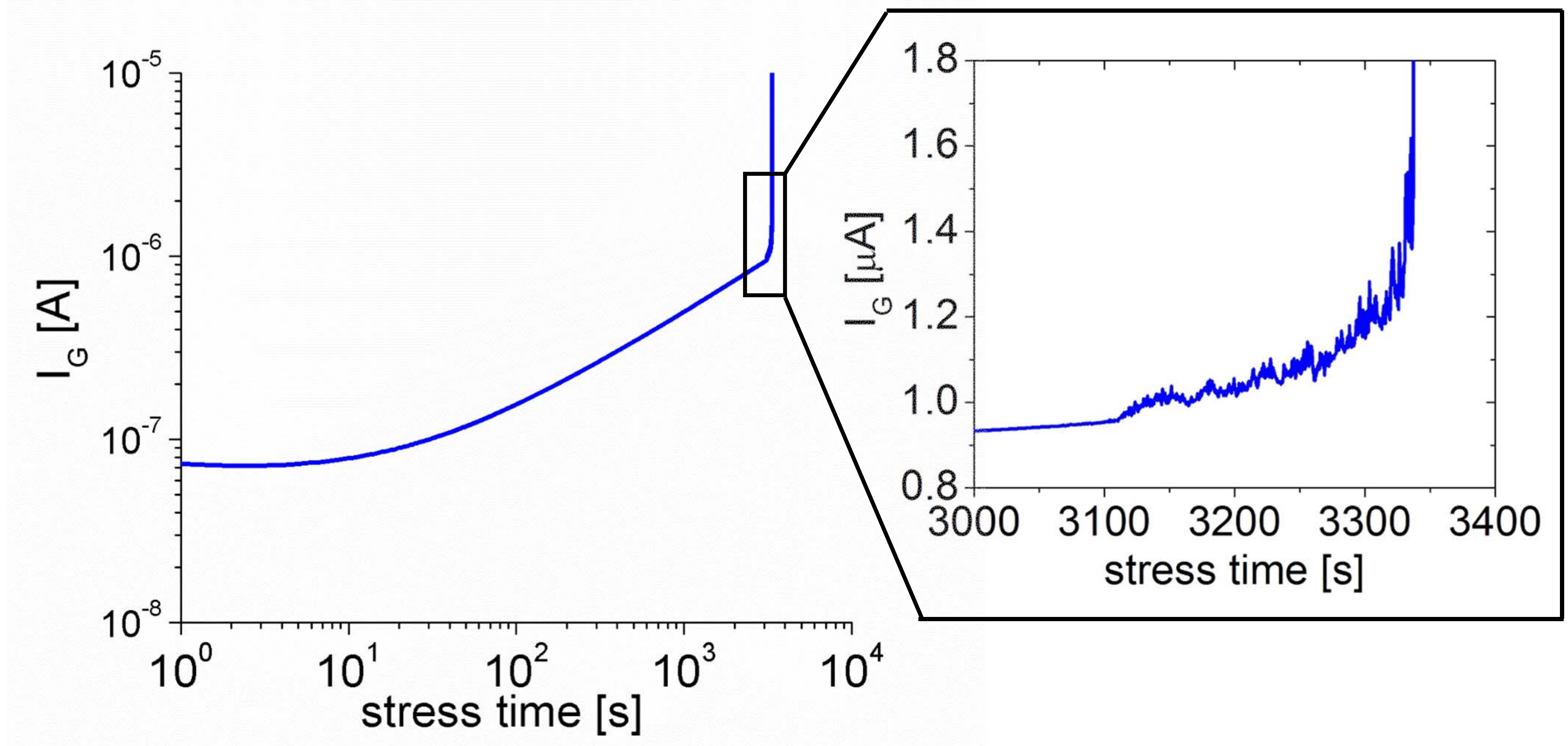

Near breakdown, I_G becomes noisy → progressive breakdown (PBD)

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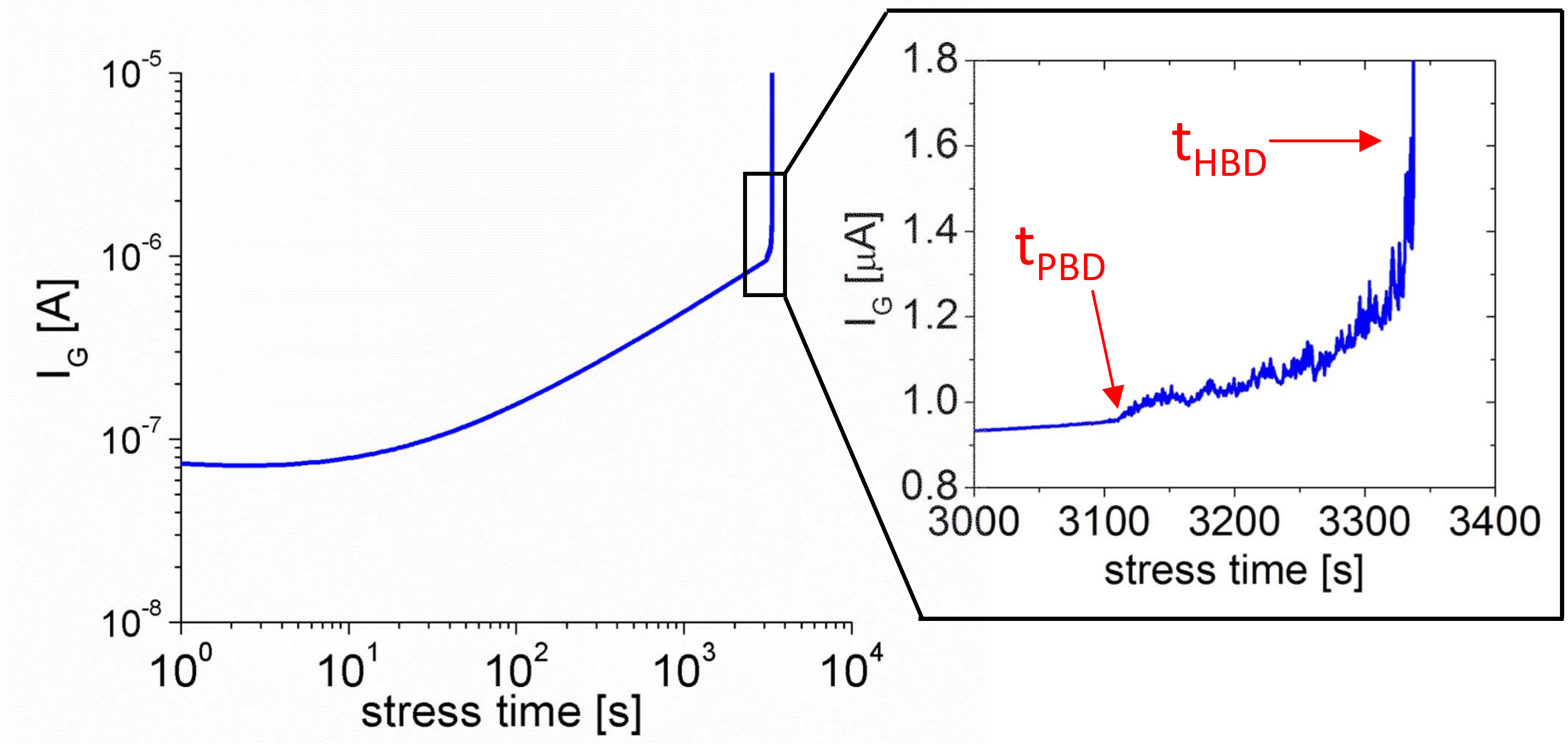

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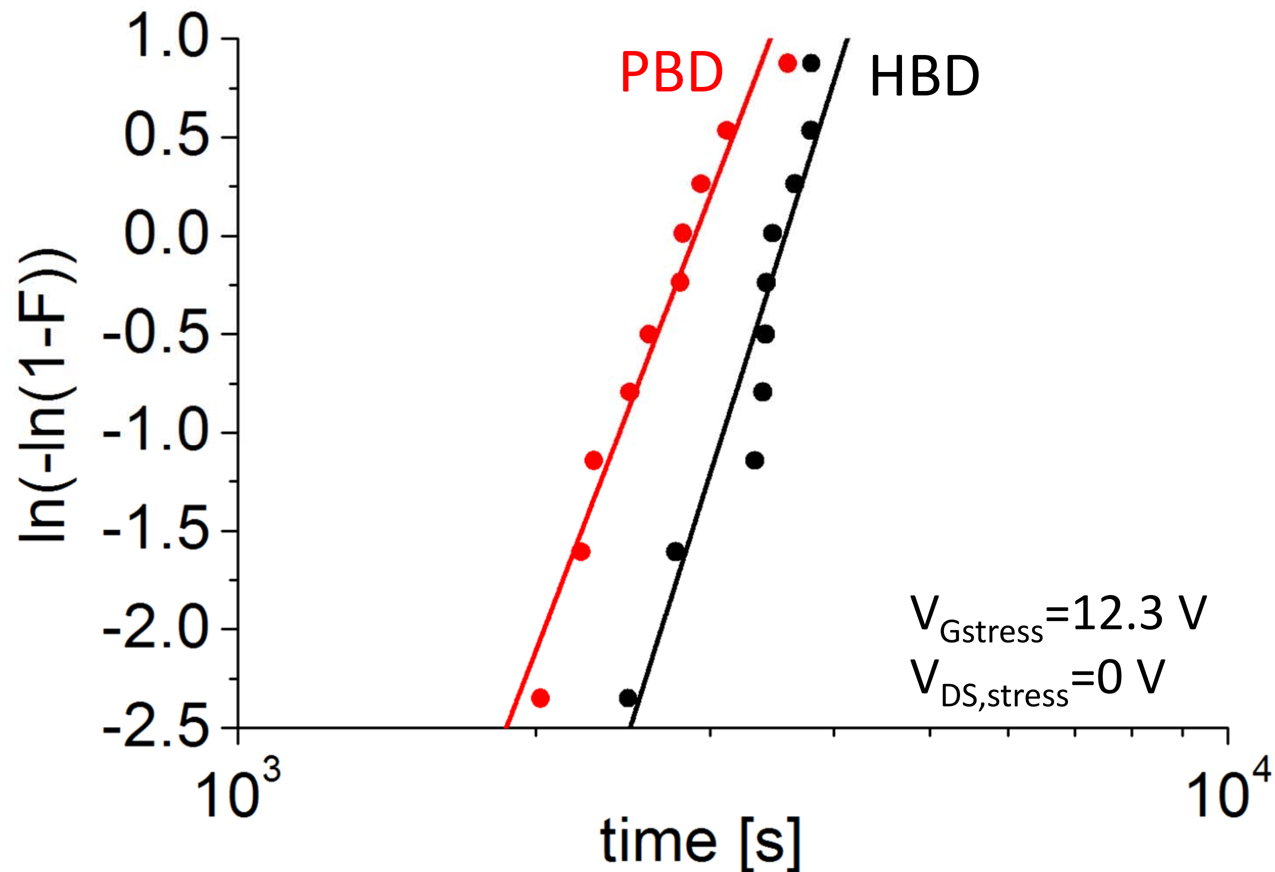
PBD Statistics

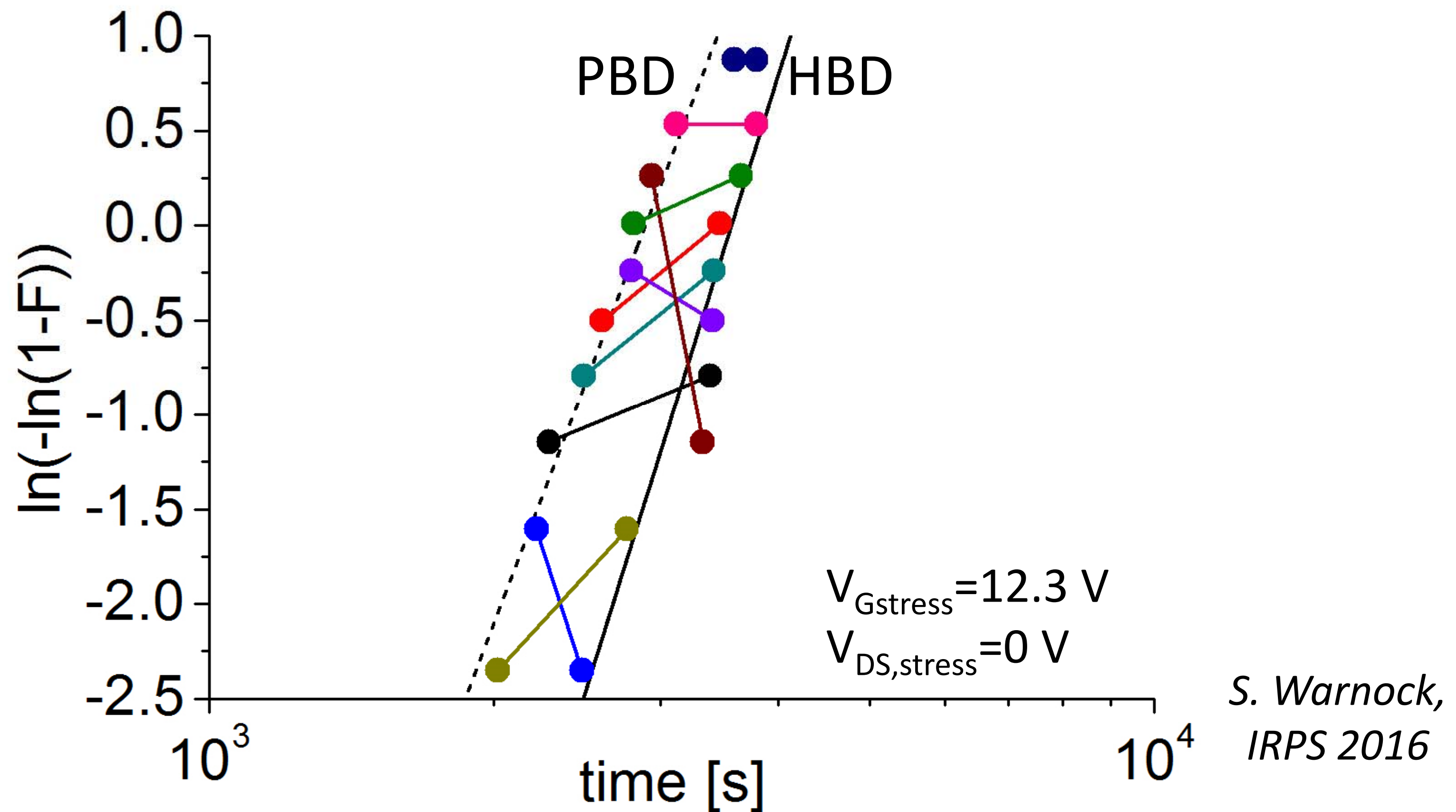
Compare statistics for t_{PBD} and t_{HBD}



Statistics nearly parallel → breakdown mechanism is same

PBD Statistics

- Examine PBD and HBD times for each individual device
- PBD and HBD in same device linked by a line



HBD, PBD uncorrelated from device to device → dielectric defect generation is truly random

Conclusions

- Developed methodology to study TDDB in GaN MIS-HEMTs
- TDDB behavior consistent with Si MOSFETs:
  - Weibull distribution
  - SILC before breakdown
  - Clear observation of Progressive Breakdown
- For moderate gate voltage stress:
  - $\Delta V_T > 0$
  - $I_G \downarrow$
- Beyond critical value of $V_{Gstress}$:
  - $\Delta V_T < 0$
  - Sudden $\Delta S \uparrow$
  - Capacitance frequency dispersion $\uparrow$

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  Onset of trap generation in dielectric/at MIS interface

Acknowledgements

Questions?